

Abstract

The present invention provides a voltage margin testing system incorporated in an electronic system, such as, a computer system (e.g., a server), having a plurality of components for at least some of which voltage margin testing is required. A voltage margin testing of the invention can include a controller, such as a Baseboard Management Controller (BMC), internal to the computer system and a digital voltage adjuster, e.g., a digital potentiometer, that is in communication with the controller. The voltage adjuster can effect generation of one or more test voltages, for example, by varying resistance in a feedback circuitry of a regulator whose output voltage is applied to system components, for application to the components in response to commands from the controller.

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